Chul Kim

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Academic Positions

2019 – present **Korea Advanced Institute of Science and Technology (KAIST)** *Daejeon, KOREA*
Assistant Professor, Department of Bio and Brain Engineering

2017 – 2019 **University of California, San Diego (UC San Diego)** *La Jolla, USA*
Postdoctoral Fellow, Department of Bioengineering
- Advisor: Prof. Gert Cauwenberghs

2012 – 2017 **University of California, San Diego (UC San Diego)** *La Jolla, USA*
Ph.D., Bioengineering
- Thesis: Energy-Efficient Integrated Biomedical Circuits and Systems for Unobtrusive Neural Recording and Wireless Body-Area Networks
- Advisor: Prof. Gert Cauwenberghs

2007 – 2009 **Korea Advanced Institute of Science and Technology (KAIST)** *Daejeon, KOREA*
M.S., Electrical Engineering
- Thesis: Design of an Amplitude Modulator for Polar Transmitters and High-gain Low-voltage Amplifiers
- Advisor: Prof. Gyu-Hyeong Cho

2000 – 2007 **Kyungpook National University (KNU)** *Daegu, KOREA*
B.S., Electrical Engineering and Computer Science
Including mandatory military service (May 2001 – July 2003)

Industry Experience

2009 – 2012 **SK Hynix Semiconductor Inc.** *Icheon, KOREA*
TSV Technology Development Team, R&D Division

- Research Projects
  - 44nm 2G double-data-rate type 3 (DDR3) memory – 3D Stacked dynamic random-access memory (DRAM) with through-silicon via (TSV) technology
  - Ultra-wide and high-speed I/O with Intel – 3D stacked DRAM with TSV technology
- Key Activities & Responsibilities
  - Design of power management units, thermal sensors, power distribution network, and TSV test circuitry for 3D stacked DRAMs
  - Training and education of analog circuit engineers (with KAIST)
  - First 16Gb 3D stacked DRAM with TSV technology

Research Experience

2012 – 2017 **University of California, San Diego** *La Jolla, USA*
Integrated Systems Neuroengineering Laboratory

- **Wireless High-density Ultra-low-power Neural Interfaces**
  DARPA NESD Program, UC Multicampus Research Programs and Initiatives (MRPI)
  - Sub-microwatt-power/channel, sub-microvolt-noise, 92dB-dynamic range, 16-channel neural recording 1 mm^2 microchip
  - Wireless power receiver and data telemetry over a single inductive link
  - Fully miniaturized autonomous system for mobile brain-machine interfaces
- **Fully Encapsulated Neural Interface and Acquisition Chip (ENIAC)**
  UC Center for Brain Activity Mapping, UC MRPI, DARPA NESD
  - The first fully integrated electrocortical brain-machine interface for 16-channel neural recording and stimulation in less than 3 mm^3 volume.
  - Integrated wireless power receiver with an on-chip inductor-capacitor tank for miniaturization of neural interfaces
  - RF-decoupling H-tree signal distribution network and resonant regulating rectifier
- **Multiple-input-multiple-output (MIMO) Radio Frequency (RF) Signal Separation and Classification Receiver**
  DARPA CLASIC Program
  - Cognitive radio and full duplex 4-channel MIMO machine-learning supportive baseband receiver
  - Capacitive spectral filter for 65 dB harmonic rejection and matrix multiplication spatial filter for 48.5 dB signal separation

2007 – 2009 **KAIST** *Daejeon, KOREA*
Circuit Design and System Application Laboratory

- **Energy-efficient RF transmission system**
  Electronics and Telecommunications Research Institute (ETRI)
  - Hybrid supply modulator for polar/envelop elimination and restoration transmitters
  - Wide bandwidth linear amplifier and energy efficient switched-mode power supply (SMPS)
- **Research intern for scholarship students**
  SK Hynix Semiconductor Inc.
  - Band-gap references in weak and strong inversion regions of MOSFET operation

Teaching Experience

"Bioengineering Laboratary I," KAIST, 2019
"Principles of Bioinstrumentation Design," Teaching Assistant, UC San Diego, 2013, 2014.
"Neurodynamics," Teaching Assistant, UC San Diego, 2014, 2015.

Journal Articles

[11] S. Joshi, **C. Kim**, C. M. Thomas, and G. Cauwenberghs, "Digitally Adaptive High-Fidelity Analog Array Signal Processing Resilient to Capacitive Multiplying DAC Inter-Stage Gain Error," in *IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS I)*, accepted.

[10] **C. Kim**, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "Sub-μV_{rms}-noise Sub-μW/Channel ADC-Direct Neural Recording with 200-mV/ms Transient Recovery Through Predictive Digital Autoranging," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 53, no. 11, pp. 3101-3110 Nov. 2018.

[9] S. Ha, **C. Kim**, J. Park, G. Cauwenberghs, and P. P. Mercier, "A Fully Integrated RF-powered Energy-replenishing Current-controlled Stimulator," in *IEEE Transactions on Biomedical Circuits and Systems*, vol. 13, no. 1, Feb. 2018.

[8] **C. Kim**, C.-S. Chae, Y.-S. Yuk, C. M. Thomas, Y.-G. Kim, J.-K. Kwon, S. Ha, G. Cauwenberghs, and G.-H. Cho, "A 500 MHz-bandwidth 7.5 mV_{PP}-ripple Power-Amplifier Supply Modulator for RF Polar Transmitters," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 53, no. 6, pp. 1653-1665, June 2018.

[7] **C. Kim**, S. Ha, J. Park, A. Akinin, P. P. Mercier and G. Cauwenberghs, "A 144 MHz Fully Integrated Resonant Regulating Rectifier with Hybrid Pulse Modulation for mm-sized Implants," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 52, no. 11, pp. 3043-3055, Nov. 2017.

[6] S. Ha, A. Akinin, J. Park, **C. Kim**, H. Wang, C. Maier, P. P. Mercier, and G. Cauwenberghs, "Silicon-Integrated High-Density Electrocortical Interfaces," in *Proceedings of the IEEE*, vol. 105, no. 1, pp. 11-33, Jan. 2017.

[5] S. Joshi, **C. Kim**, G. Cauwenberghs, "A 6.5μW/MHz Charge Buffer With 7-fF Input Capacitance in 65-nm CMOS for Noncontact Electropotential Sensing," in *IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS II)*, vol. 63, no. 12, pp. 1161-1165, Dec. 2016.

[4] S. Ha, **C. Kim**, J. Park, S. Joshi, and G. Cauwenberghs, "Energy-Recycling Telemetry IC with Simultaneous 11.5-mW Power and 6.78-Mbps Backward Data Delivery over a Single 13.56-MHz Inductive Link," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 11, pp. 2664-2678, Nov. 2016.

[3] **C. Kim**, S. Joshi, C. M. Thomas, S. Ha, L. E. Larson and G. Cauwenberghs, "A 1.3 mW 48 MHz 4 Channel MIMO Baseband Receiver With 65 dB Harmonic Rejection and 48.5 dB Spatial Signal Separation," in *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 51, no. 4, pp. 832-844, Apr. 2016.

[2] S. Ha, **C. Kim**, Y.M. Chi, A. Akinin, C. Maier, A. Ueno, G. Cauwenberghs, "Integrated Circuits and Electrode Interfaces for Noninvasive Physiological Monitoring," in *IEEE Transactions on Biomedical Engineering (TBME),* vol. 61, no. 5, pp.1522-1537, May 2014.

[1] Y.S. Yuk, S.-C Jung, **C. Kim**, H.-D Gwon, S. Choi, G.-H. Cho, "PSR Enhancement Through Super Gain Boosting and Differential Feed-Forward Noise Cancellation in a 65-nm CMOS LDO Regulator," *IEEE Transactions on Very Large Scale Integration (TVLSI) Systems,* pp.1-11, Nov. 2013.

Peer-reviewed Conference Proceedings

[17] **C. Kim**, S. Joshi, H. Courellis, J. Wang, C. Miller, and G. Cauwenberghs, "A 92dB dynamic range sub–μVrms noise 0.8μW/ch neural recording ADC array with predictive digital autoranging," *2018 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, Feb. 2018.

[16] J. Park, **C. Kim**, A. Akinin, S. Ha, G. Cauwenberghs, and P. P. Mercier, "Wireless Powering of mm-scale Fully-on-chip Neural Interfaces," *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, Oct. 2017 (*Invited Paper*).

[15] **C. Kim**, S. Ha, A. Akinin, J. Park, R. Kubendran, H. Wang, P. P. Mercier, and G. Cauwenberghs, "Design of Miniaturized Wireless Power Receivers for mm-sized Implants," *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, pp. 1-8, Apr. 2017 (*Invited Paper*).

[14] S. Joshi, **C. Kim**, S. Ha, and G. Cauwenberghs, "From Algorithms to Devices: Enabling Machine Learning through Ultra-Low-Power VLSI Mixed-Signal Array Processing," *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, pp. 1-9, Apr. 2017 (*Invited Paper*).

[13] S. Joshi, **C. Kim**, S. Ha, Y. M. Chi and G. Cauwenberghs, "2pJ/MAC 14b 8×8 linear transform mixed-signal spatial filter in 65nm CMOS with 84dB interference suppression," *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 364-365, Feb. 2017.

[12] **C. Kim**, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier and G. Cauwenberghs, "A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution," *2016 Symposium on VLSI Circuits*, Kyoto, June 2016.

[11] S. Joshi, **C. Kim**, and G. Cauwenberghs, "A 6μW/MHz charge buffer with 7fF input capacitance in 65nm CMOS for non-contact electropotential sensing," *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2907-2907, May 2016.

[10] **C. Kim**, S. Ha, J. Park, A. Akinin, P. P. Mercier and G. Cauwenberghs, "A 144MHz integrated resonant regulating rectifier with hybrid pulse modulation," *2015 Symposium on VLSI Circuits*, Kyoto, pp. C284-C285, Jun. 2015.

[9] **C. Kim**, S. Joshi, C. M. Thomas, S. Ha, A. Akinin, L. E. Larson, and G. Cauwenberghs, "A CMOS 4-channel MIMO baseband receiver with 65dB harmonic rejection over 48MHz and 50dB spatial signal separation over 3MHz at 1.3mW," *2015 Symposium on VLSI Circuits*, Kyoto, pp. C304-C305, Jun. 2015.

[8] S. Ha, A. Akinin, J. Park, **C. Kim**, H. Wang, C. Maier, G. Cauwenberghs, and P.P. Mercier, "A 16-channel wireless neural interfacing SoC with RF-powered energy-replenishing adiabatic stimulation," *2015 Symposium on VLSI Circuits*, Kyoto, pp. C106-C107, Jun. 2015.

[7] **C. Kim**, S. Ha, C. M. Thomas, S. Joshi, J. Park, L. E. Larson, and G. Cauwenberghs, "A 7.86 mW +12.5 dBm In-Band IIP3 8-to-320 MHz Capacitive Harmonic Rejection Mixer in 65nm CMOS," *Proceedings of the ESSCIRC*, Sep. 2014.

[6] S. Ha, **C. Kim**, J. Park, S. Joshi and G. Cauwenberghs, "Energy-Recycling Integrated 6.78-Mbps Data 6.3-mW Power Telemetry over a Single 13.56-MHz Inductive Link," 2014 Symposium on *VLSI Circuits*, pp. 53-54, Jun. 2014.

[5] J. Park, S. Ha, **C. Kim**, S. Joshi, T. Yu, W. Ma and G. Cauwenberghs, "A 12.6 mW 8.3 Mevents/s contrast detection 128×128 imager with 75 dB intra-scene DR asynchronous random-access digital readout," *2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings*, Lausanne, pp. 564-567, Oct. 2014.

[4] Y. S. Yuk, S.-C Jung, B. Lee, S.-W. Wang, **C. Kim**, G.-H. Cho, "A CMOS LDO regulator with high PSR using Gain Boost-Up and Differential Feed Forward Noise Cancellation in 65nm process," *Proceedings of the ESSCIRC*, pp.462-465, Sep. 2012.

[3] J.-C. Lee, S.-H. Jin, D.-S. Kim, Y.-J. Ku, **C. Kim**, B.-K. Park, H.-G. Kim, S.-J. Ahn, J.-J. Lee, S.-J. Hong, "A Low-Power Small-Area Open Loop Digital DLL for 2.2Gb/s/pin 2Gb DDR3 SDRAM," *IEEE Asian Solid-State Circuits Conference (A-SSCC),* pp. 14-16, Nov. 2011.

[2] **C. Kim**, C.-S. Chae, Y.-S. Yuk, Y.-G. Kim, J.-K. Kwon, G.-H. Cho, "A 105dB-Gain 500MHz-Bandwidth 0.1Ω-Output-Impedance Amplifier for an Amplitude Modulator in 65nm CMOS," *2010 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, pp. 88-89, Feb. 2010.

[1] T.-W. Kwak, M.-C. Lee, Y.-S. Yuk, K.-H. Lee, H.-H. Park, **C. Kim**, G.-H. Cho, "Hybrid Switching Amplifier Using a Novel Two Quadrant Wideband Buffer for Dynamic Power Supply Applications," IEEE *Power Electronics Specialists Conference (PESC)*, pp. 546-551, Jun. 2008.

Patents

[8] **C. Kim**, G. Cauwenberghs, P. P. Mercier, S. Ha, J. Park, A. Akinin, "Resonant regulating rectifier with an integrated antenna" US Patent App., 15/736,239, Jul., 2018.

[7] S. Ha, G. Cauwenberghs, **C. Kim**, J. Park, P. P. Mercier, A. Akinin, H. Wang, C. Maier, "Radio frequency powered adiabatic stimulation with energy replenishment" US Patent App., 15/736,252, Jun., 2018.

[6] **C. Kim**, C. M. Thomas, G. Cauwenberghs, L. E. Larson, S. Joshi, S. Ha, "Capacitive Passive Mixer Baseband Receiver with Broadband Harmonic Rejection" US Patent, Patent Number 9,876,518 May, 2017.

[5] **C. Kim**, J. Lee, "Semiconductor Circuit," US Patent, Patent Number 8,159,261, Apr. 2012 China Patent, Application No. 201010216191.7, Jul. 2010, and Taiwan Patent, Application No. 99140048, Nov. 2010.

[4] D. Kim, J. Lee, **C. Kim**, "Integrated Circuit for Detecting Defects of Through Chip Via," US Patent, Patent Number 8,976,869, Feb. 2015. China Patent, Application No. 201110130233.X, May 2011, and Taiwan Patent, Application No. 100108584, Mar 2011.

[3] **C. Kim**, J. Lee, "Semiconductor Memory Apparatus," US Patent, Patent Number 8,411,512, Apr. 2013.

[2] **C. Kim**, "Semiconductor Device and Operating Method Thereof", US Patent, Patent Number 8,330,533, Dec. 2012.

[1] **C. Kim**, "Impedance Calibration Apparatus of Semiconductor Integrated Circuit," US Patent, Patent Number 9,374,088, June 2016.

Books and Book Chapters

S. Ha, **C. Kim**, P.P. Mercier, G. Cauwenberghs, *High-Density Integrated Electrocortical Neural Interfaces*, Elsevier, will be published in Sep. 2019.
S. Ha, **C. Kim**, Y.M. Chi, G. Cauwenberghs, "Low power integrated circuit design for wearable biopotential sensing," in E. Sazonov and M. R. Neuman, *Wearable sensors: Fundamentals, implementation and applications* Academic Press, 1st edition, Sep. 2014.

Invited Talks

"High-Density Integrated Conformal Electrocortical Neural Interfaces for Neurological Electroceuticals" KAIST, South Korea, Nov. 2018.

"Energy-Efficient Integrated Biomedical Circuits and Systems for Unobtrusive Neural Recording and Wireless Body-Area Networks" Boston University, Mar., 2018, Virginia Tech, Apr. 2018; University of Waterloo, Apr. 2018; *IEEE International SoC Design Conference*, Daegu, South Korea, Nov. 2018.

"Design of Miniaturized Wireless Power Receivers for mm-sized Implants" *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, Apr. 2017.

Awards

Predoctoral Achievement Award for 2017-18, IEEE Solid-State Circuits Society
Shunichi Usami Ph.D. Thesis Design Award, 2017-18, UC San Diego Bioengineering
Gold Medal (First Prize), 16th Samsung Electronics Humantech Thesis Prize Contest
Grand Prize, 2007 Undergraduate Graduation Research Competition at EECS, KNU

Editorial Activities

Reviewer for:
IEEE Transaction on biomedical Circuits and Systems (TBioCAS)
IEEE Journal of Solid-State Circuits (JSSC)
IEEE Transaction on Power Electronics (TPEL)
IEEE Reviews in Biomedical Engineering (RBME)
IEEE Biomedical Circuits and Systems Conference (BioCAS)
IEEE International Symposium on Circuits and Systems (ISCAS)